

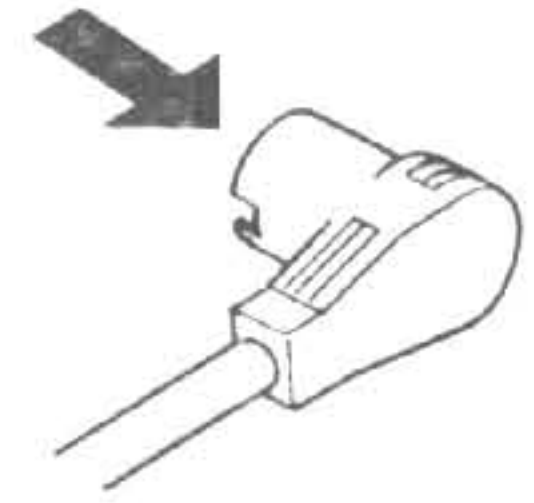
# 5. SCHEMATIC CIRCUIT DIAGRAM

A

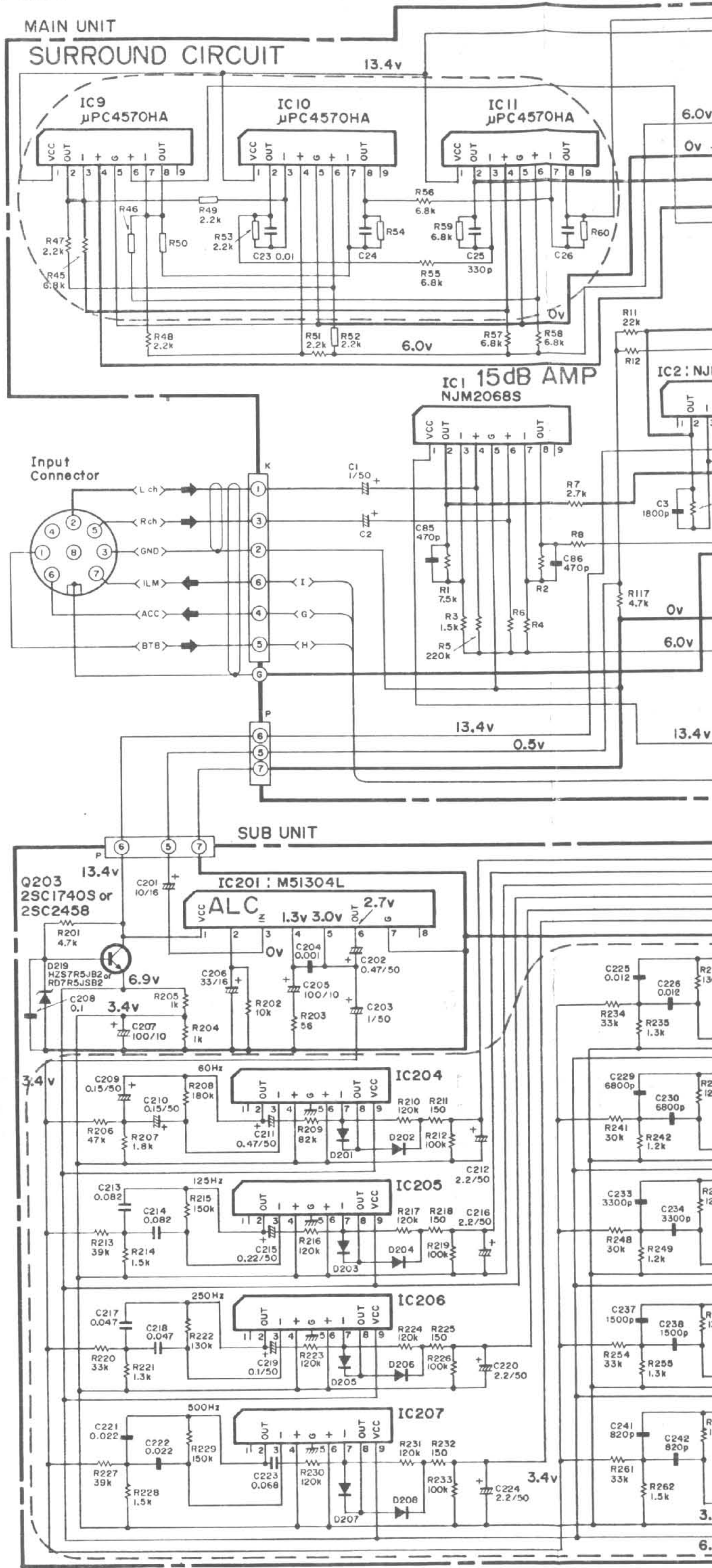
B

C

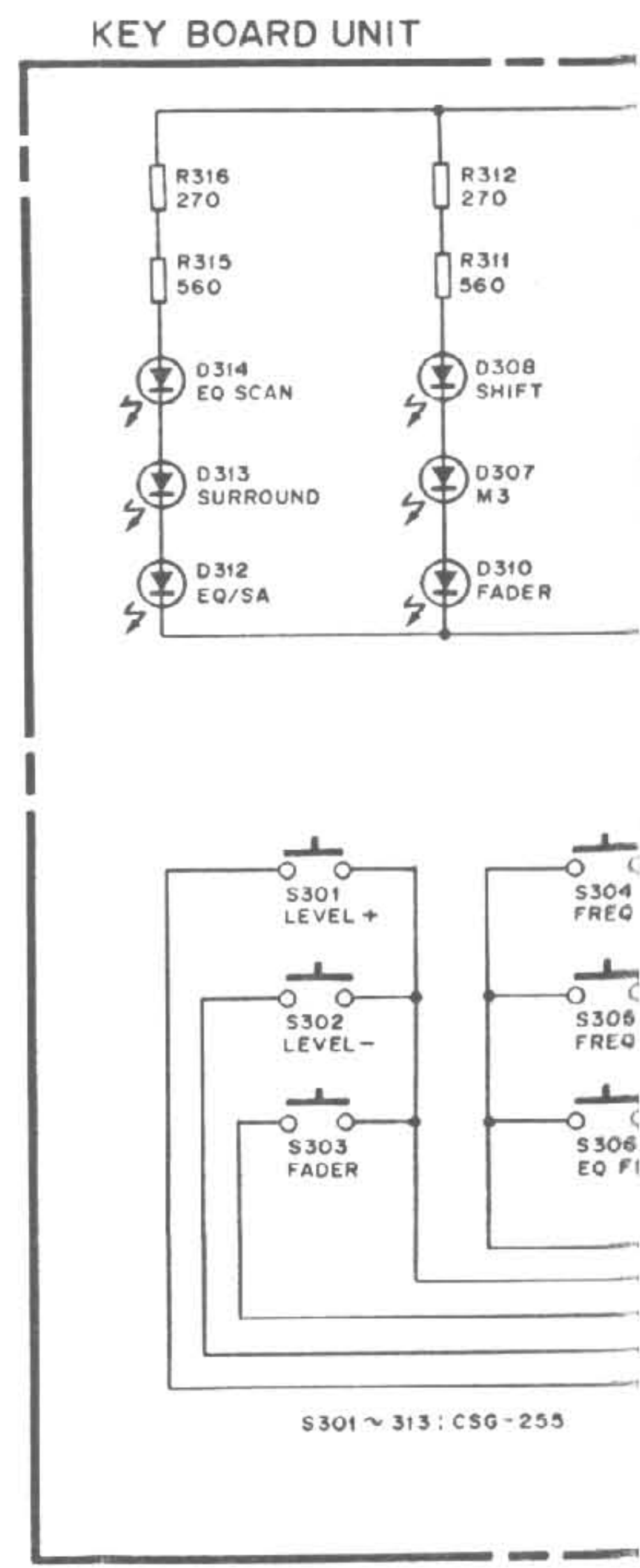
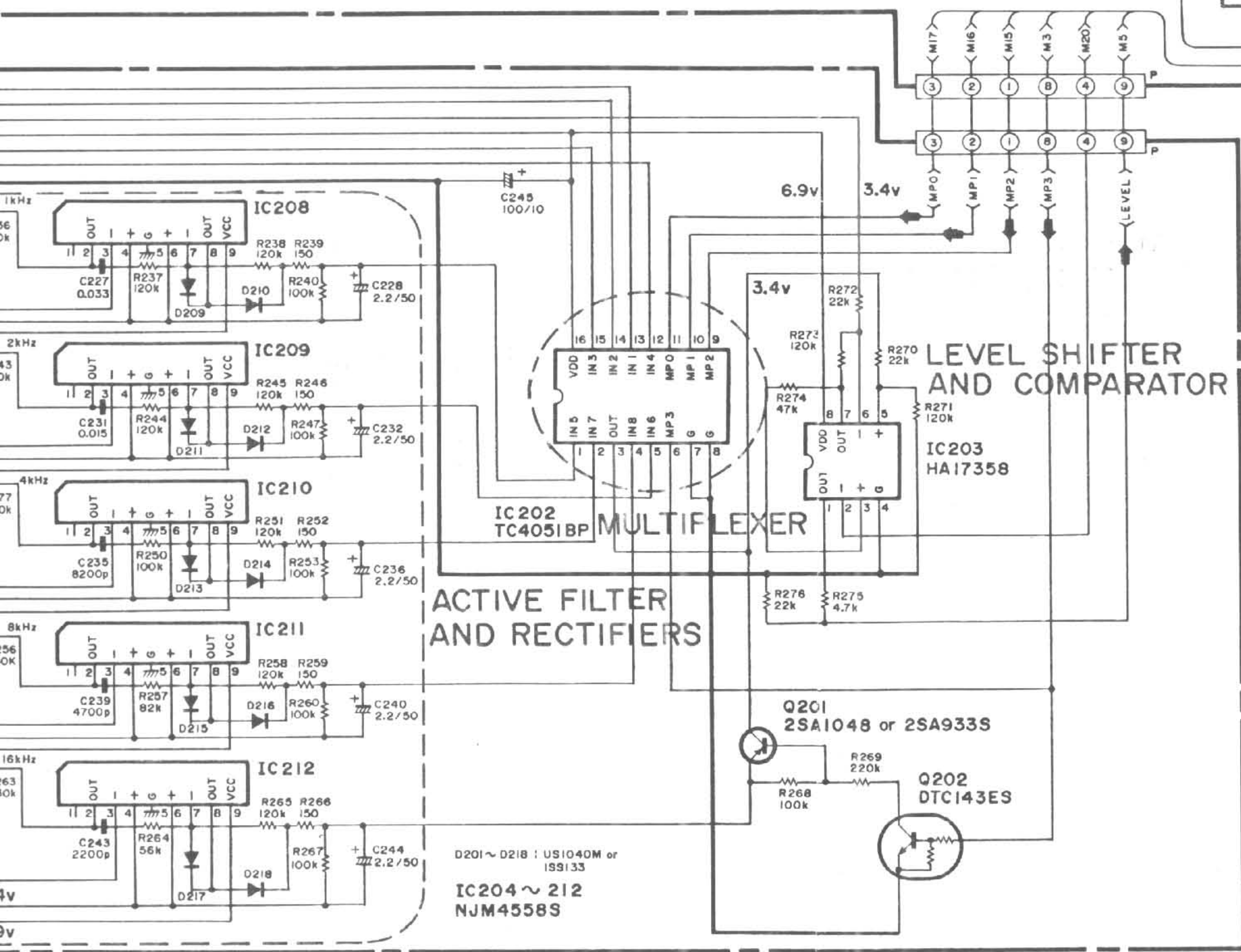
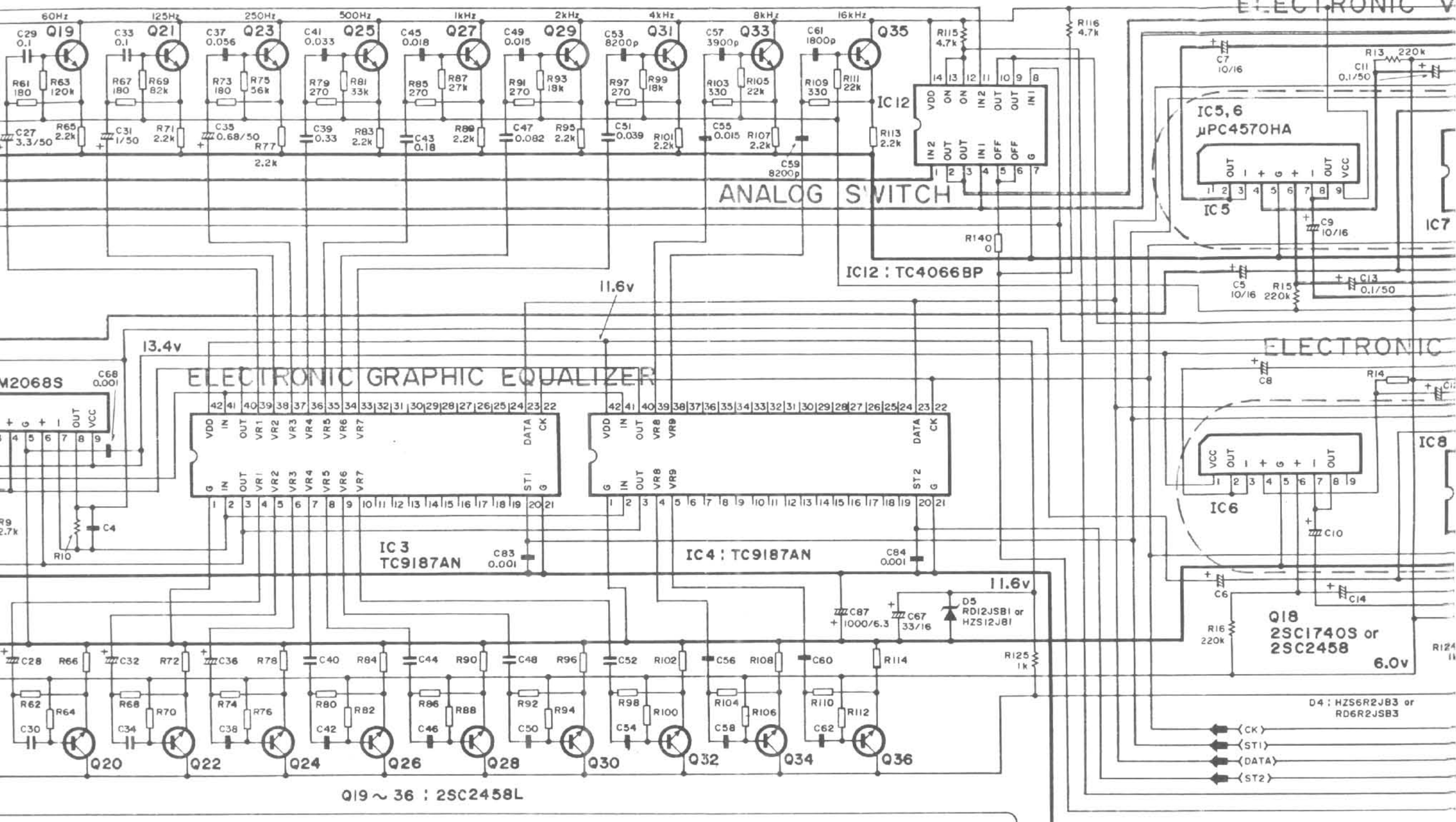
D



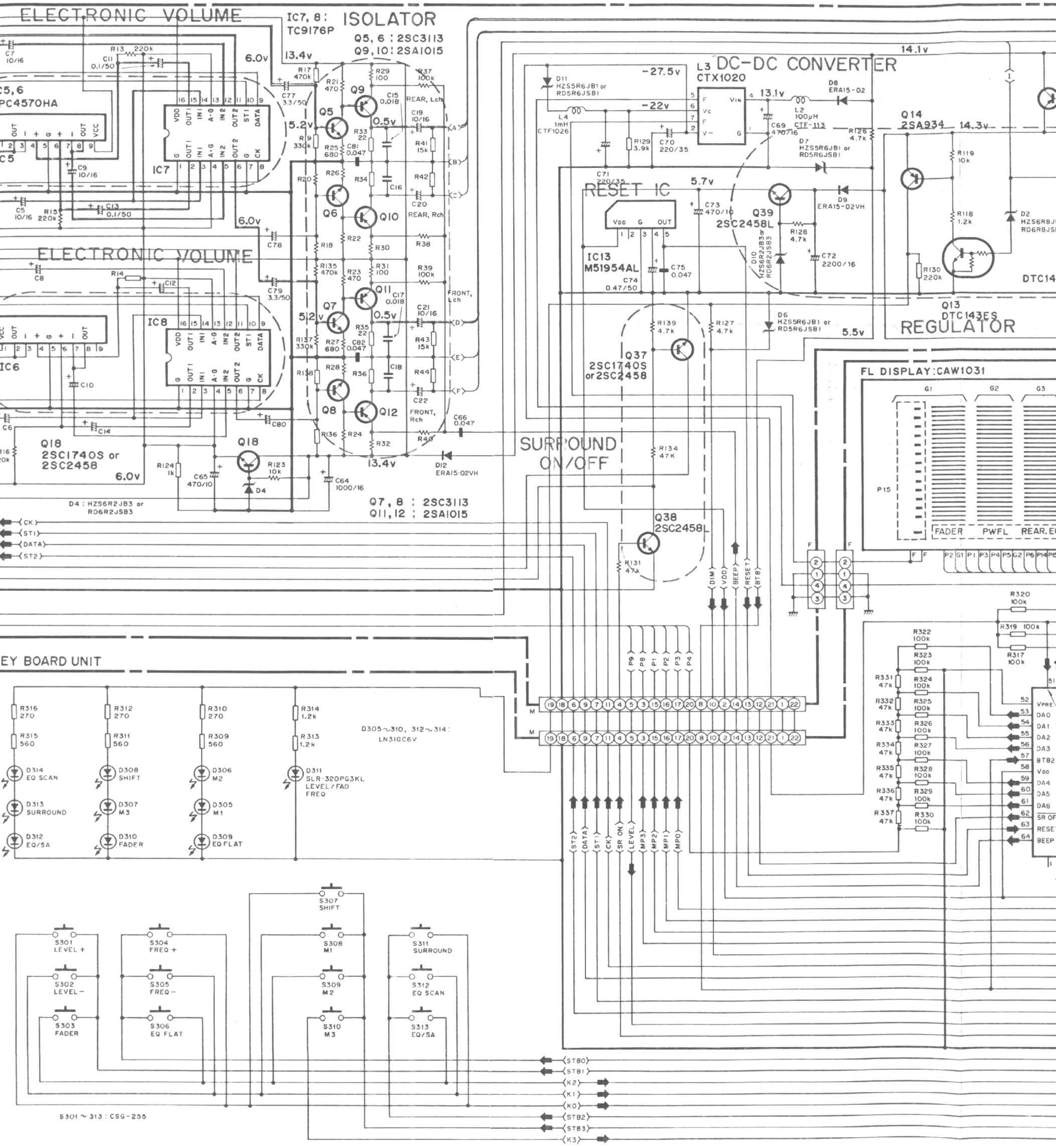
The view of the connector is one seen from the mating connector.



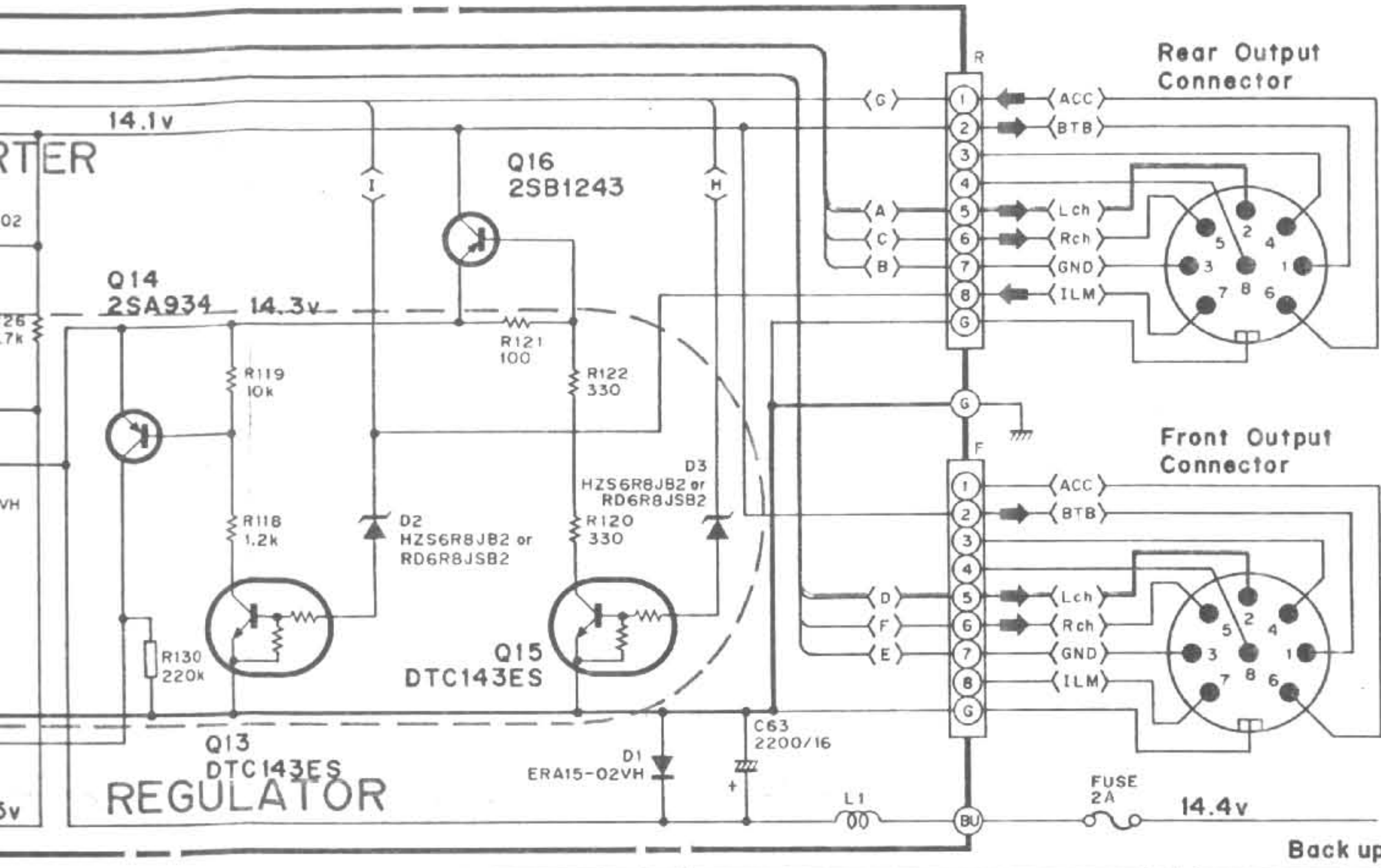






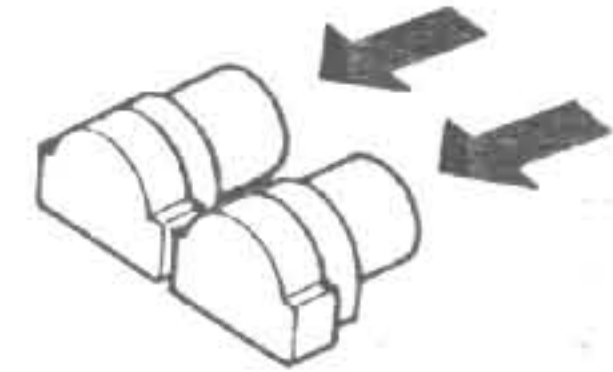




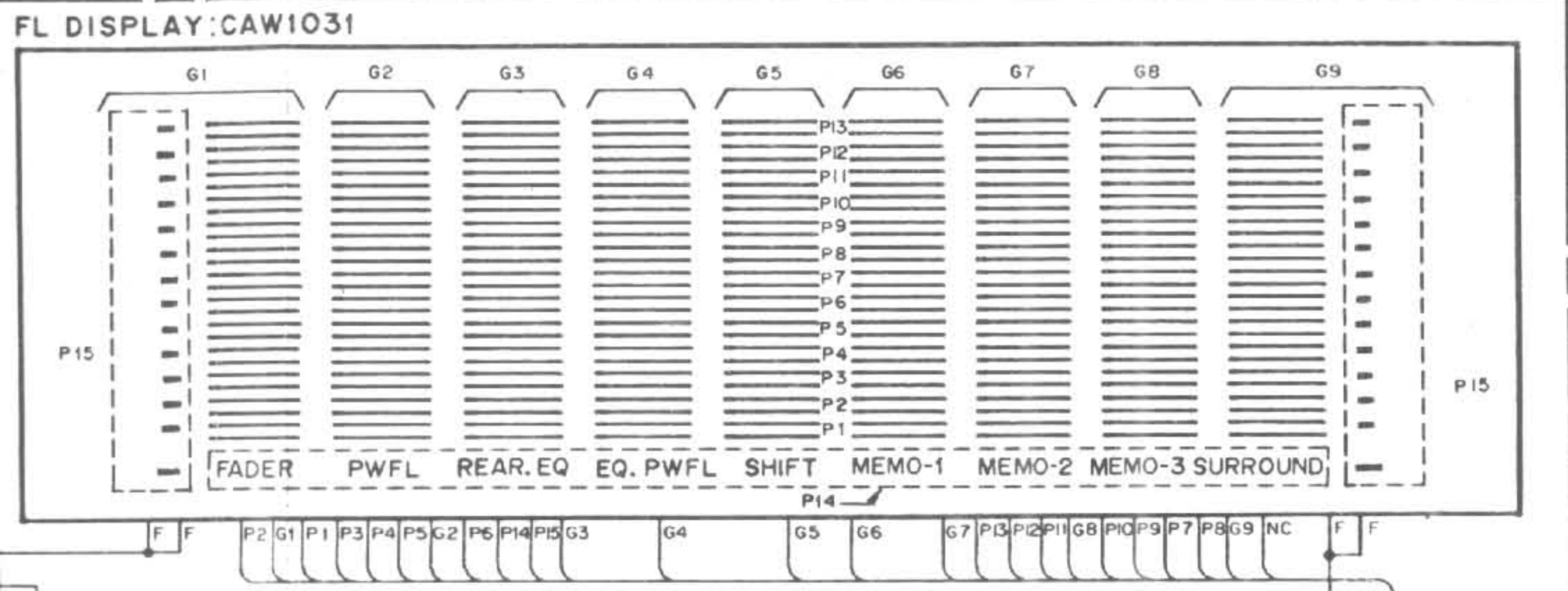


NOTE:

- Indicates a chip resistor
- Indicates a chip capacitor
- Indicates a chip diode



The view of the connector is one seen from the mating connector.



**Graphic Equalizer Assy**

Consists of

- Main Unit
- Sub Unit

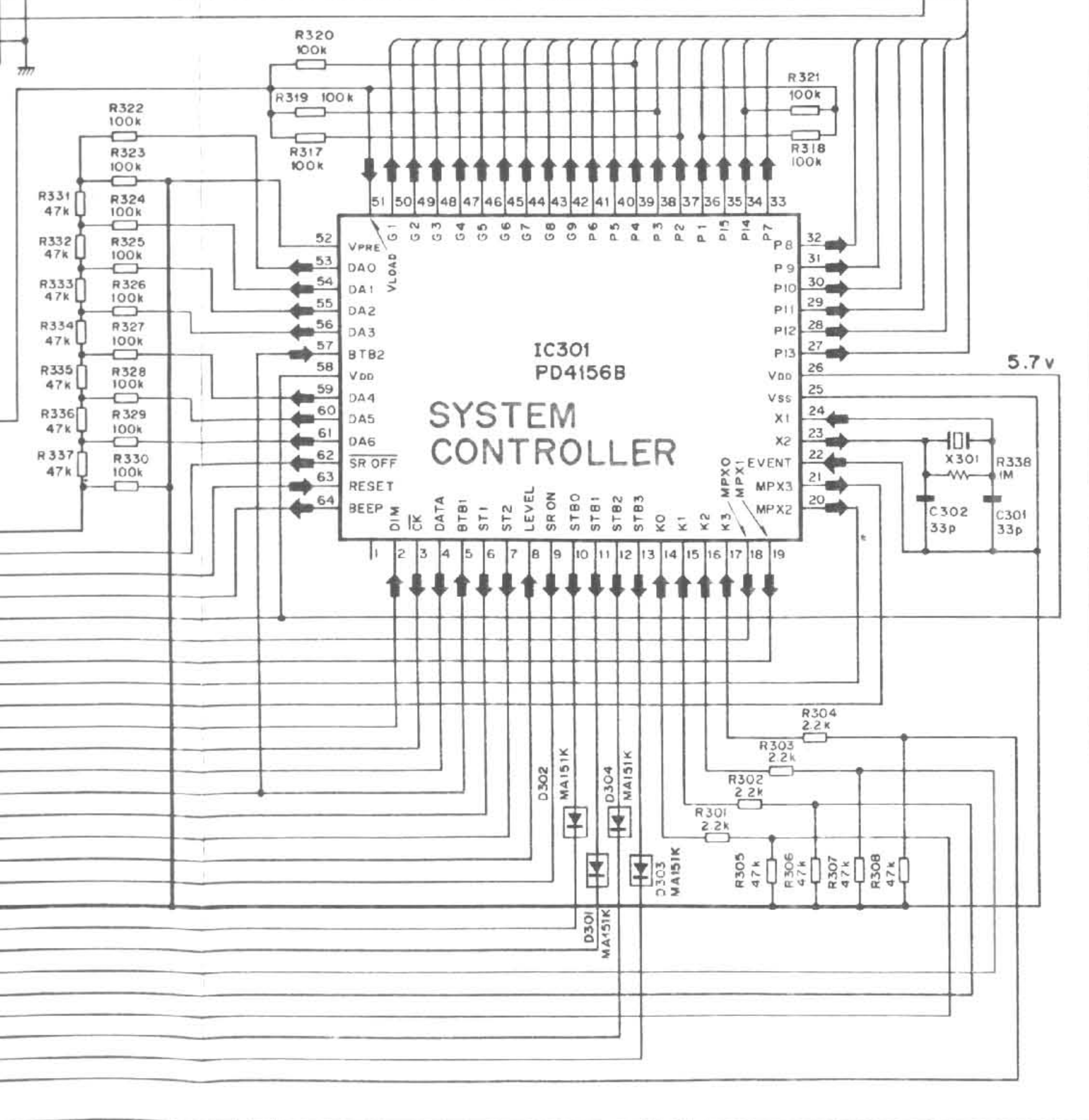
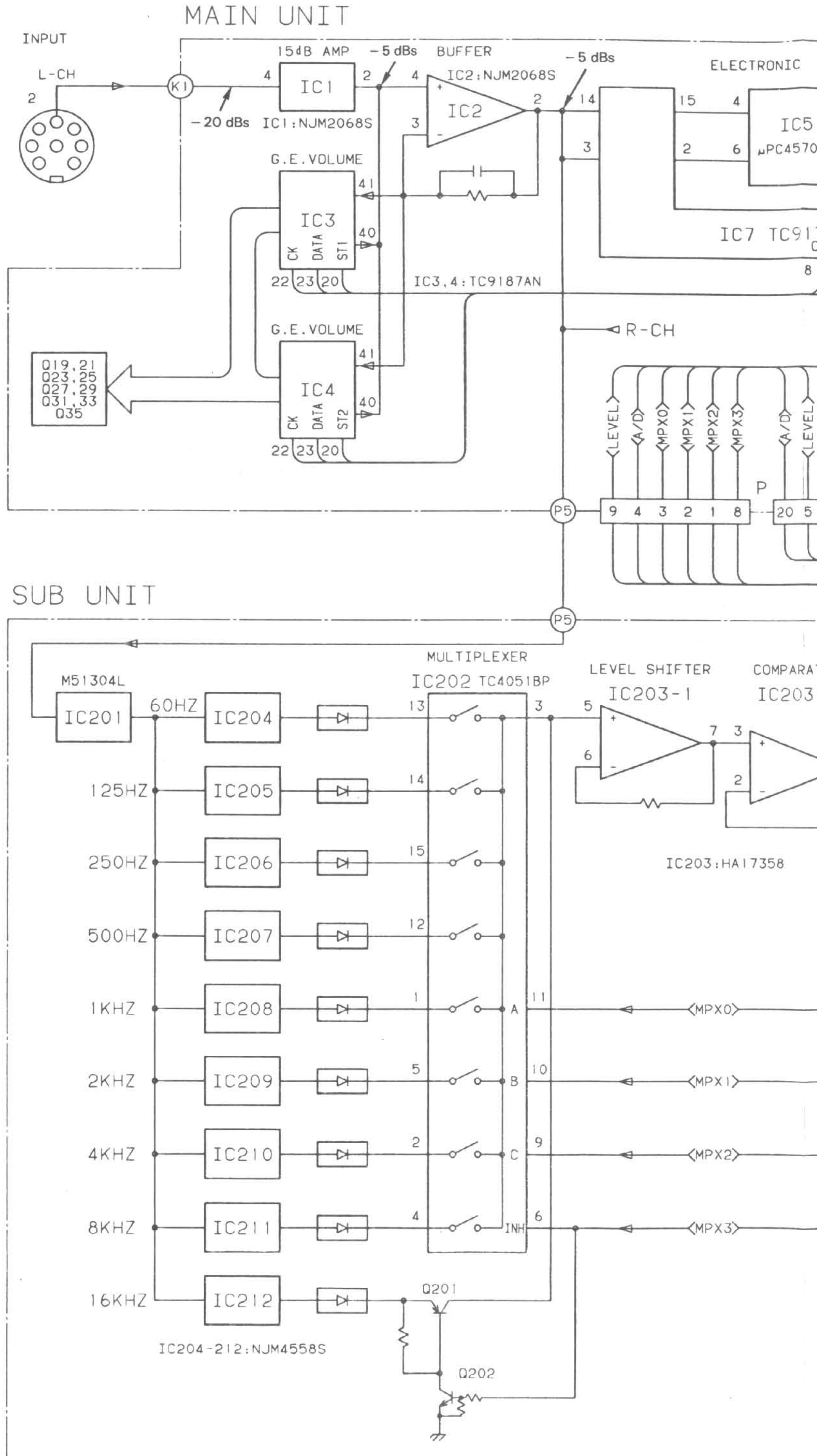


Fig. 6



# 4. BLOCK DIAGRAM



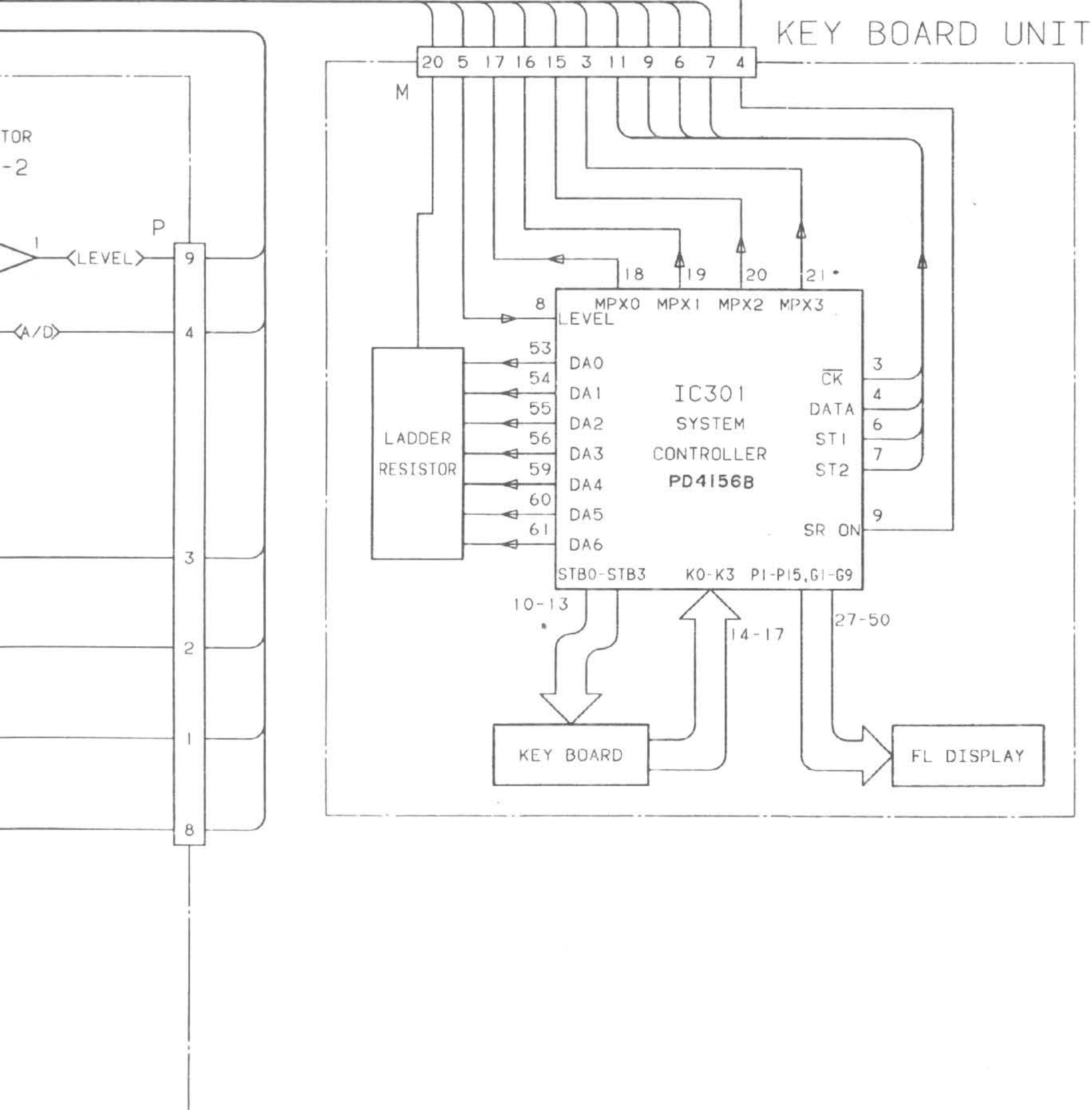
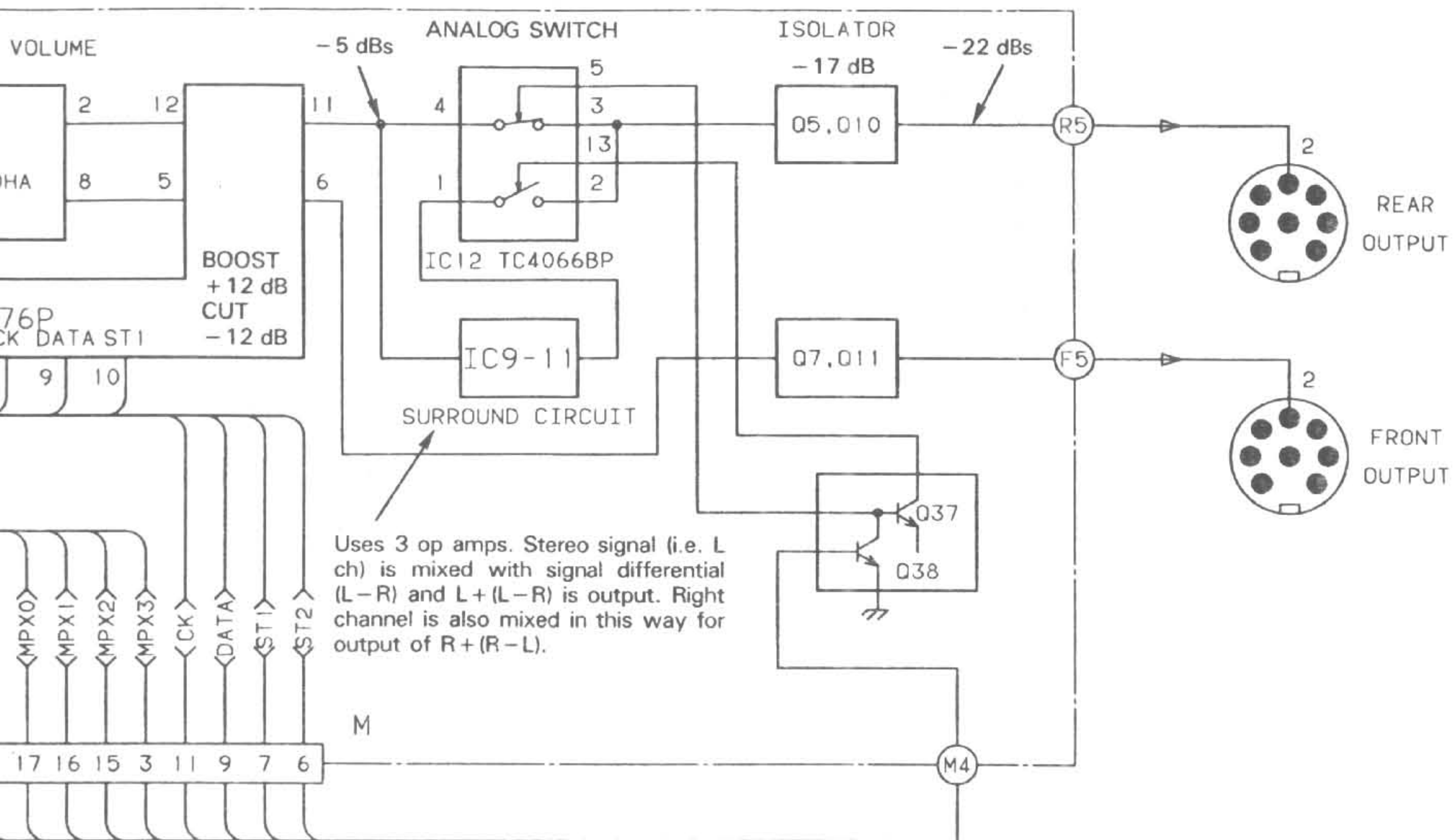


Fig. 5